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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,863	08/28/2003	Simar Maangat	ALT-276	1004

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/652,863	MAANGAT, SIMAR	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 20-40* is/are allowed.

6)☒ Claim(s) *1,2,4-7,10,12-18 and 41* is/are rejected.

7)☒ Claim(s) *3,8,9 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Tammone, Jr. (U.S. Patent No. 6,313,997).

In reference to claim 41, Tammone discloses in Figure 1 an electrical circuit comprising: means (base terminals of transistors Q1 and Q2) for receiving differential electrical signals (VIN_n, VIN_p), one of the differential signals being at a high voltage and the other of the differential signals being at a low voltage; means (Q1, Q2, R1, R2, Q3, Q4) for producing output signal transitions in response to transitions of the differential signals (VIN_n, VIN_p); capacitance means (C1, C2) for boosting the transition speed of the output signal transitions; and means (Q5, Q6) for selecting the amount of the capacitance means with which to boost the transition speed. The same applies to claims 1 and 2.

3. Claims 4-7, 10, and 12-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Rastegar (U.S. Patent No. 6,356,135).

In reference to claim 12 Rastegar discloses in Figure 4 equalization circuitry comprising: a first node (14) at which a current-flow transitions from low current to high current occurs in response to a voltage transition of a first signal (this is seen to occur in

connection with the amplifier 1 shown in Figure 3 to which the programmable capacitance circuit 10 is connected); a second node (16) at which a current-flow occurs in response to a transition of a second signal voltage (this is seen to occur in connection with the amplifier 1 shown in Figure 3 to which the programmable capacitance circuit 10 is connected); a first series connection of a first switch (34), a capacitance (32), and a second switch (34) coupled in series between the first (14) and second (16) nodes, the first and second switches (34) opening substantially simultaneously and closing substantially simultaneously; and a second series connection of a first switch (34), a capacitance (32), and a second switch (34) coupled in series between the first (14) and second (16) nodes, the second series first and second switches (34) opening substantially simultaneously and closing substantially simultaneously; wherein the first and second series connections are coupled in parallel with respect to each other between the first (14) and second (16) nodes. The same applies to claims 1-2, 4, 5 (wherein Figure 4 further shows a third selectable capacitance operative to boost the transition speed of the differential signals, received by amplifier 1 of Figure 3, in combination with the first and second selectable capacitances), 6-7, and 10.

In reference to claim 13, Rastegar discloses in Figure 4 that the capacitance consists of capacitors (32).

In reference to claim 14, Rastegar discloses in column 4, lines 64-67 that the switches may comprise solid state MOSFET devices (wherein the connection is seen to be obvious and it is well-known that depending on layout N-channel and P-channel MOSFETs can be used interchangeably).

In reference to claim 15, although Rastegar does not specifically disclose the printed circuit board for mounting the circuit of Figure 4, he does disclose (in column 1, lines 27-32) that it can be used in many electronic circuits (wherein the choice of using a printed circuit board is seen to be a design expedient dependent on the particular environment).

In reference to claim 16, Rastegar discloses in Figure 4 a memory (38).

In reference to claim 17, Rastegar discloses in Figure 4 processing circuitry (36).

In reference to claim 18, Rastegar discloses in Figure 4 a digital processing system comprising: a processor (36); a memory (38) coupled to the processor (36); and the equalization circuitry coupled to at least one of the processor (36) and the memory (38).

Allowable Subject Matter

4. Claims 11 and 20-40 are allowed.

5. Claims 3, 8-9, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Claims 3 and 8-9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 7 wherein the circuit includes two integrated circuit capacitance devices (734, 736) coupled in series to each other in combination with the rest of the limitations of the base claims and any intervening claims. Claim 19 would be allowable because the closest prior art of record fails to disclose a circuit as

shown in Figure 9 wherein at least one of the processor (944) and the memory (946) comprises the equalization circuitry in combination with the rest of the limitations of the base claims and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Claims 11 and 20-40 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 7 wherein the circuit includes two series-coupled capacitance devices (734, 736) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

May 27, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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